What is claimed is:

1. A method of manufacturing a stacked-gate flash memory, comprising:

forming a first dielectric layer on a semiconductor substrate as a tunneling dielectric;

forming a first conductive layer on said first dielectric layer;

patterning said first dielectric layer, said first conductive layer and said substrate to form a trench in said substrate;

forming an isolation into said trench;

removing a portion of said isolation to a surface of said first conductive layer;

removing a portion of said first conductive layer, thereby forming a cavity between two of said isolation;

forming a second conductive layer along a surface of said cavity and said isolation;

removing a portion of said second conductive layer to a surface of said isolation, wherein said second conductive layer and said first conductive layer act as a floating gate;

forming a second dielectric layer on a surface of said floating gate; and

forming a third conductive layer on said second dielectric layer as a control gate.

2.The method of Claim 1, wherein said isolation is removed by chemical mechanical polishing.

3. The method of Claim 1, wherein said first conductive layer is removed by high selectivity etching.

4. The method of Claim 1, wherein said second conductive layer is removed by chemical mechanical polishing.

5. The method of Claim 1, wherein said first dielectric layer comprises oxide.

6. The method of Claim 1, wherein said isolation comprises oxide.

7. The method of Claim 1, wherein said second dielectric layer comprises oxide/nitride.

8. The method of Claim 1, wherein said second dielectric layer comprises oxide/nitride/oxide.

9. The method of Claim 1, wherein said first conductive layer comprises polysilicon.

10. The method of Claim 1, wherein said second conductive layer comprises polysilicon.

11. The method of Claim 1, wherein said third conductive layer comprises polysilicon.

12. A stacked-gate flash memory comprising:

a substrate having a trench formed therein;

a tunneling oxide formed on a surface of said substrate and adjacent to said trench;

a first part of a floating gate formed on said tunneling gate;

a raised isolation filler formed in said trench and protruding over an upper surface of said first part of said floating gate, thereby forming a cavity between two adjacent raised isolation filler;

a second part of said floating gate formed along a surface of said cavity to have a U-shaped structure in cross sectional view, wherein the high level of said U-shaped structure is the same with the one of said raised isolation filler;

a dielectric layer conformally formed on a surface of said second part of said floating gate; and

a control gate formed on said dielectric layer.

13.The stacked-gate flash memory of Claim 12, wherein said raised isolation filler includes oxide.

14.The stacked-gate flash memory of Claim 12, wherein said first part of said floating gate includes polysilicon.

15.The stacked-gate flash memory of Claim 12, wherein said second part of said floating gate includes polysilicon.

16.The stacked-gate flash memory of Claim 12, wherein said dielectric layer includes oxide/nitride/oxide.

17.The stacked-gate flash memory of Claim 12, wherein said dielectric layer includes oxide/nitride.